

CA-IS23050W Precision 120kHz Hall-Effect Current Sensor with 5kV_{RMS} Reinforced Isolation Voltage and Zero Current Output Voltage Reference

1. Features

- Differential hall sensing rejects common-mode fields and nearly zero magnetic hysteresis
- Integrated digital temperature compensation circuitry allows for near closed loop accuracy
- High immunity to external magnetic fields
- Precision zero-current reference output
- Primary conductor resistance: $0.61m\Omega$
- High current sense range capability: ±50A_{PK}
- High accuracy
 - Total output error: ±3% Max@25°C to +125°C
 - Total output error lifetime drift: ±5% Max
 - Sensitivity error: ±2.5% Max@25°C to +125°C
 - Non-linearity: ±1% Max
 - Symmetry: $\pm 1\%$ Max
- Fast response
 - Signal bandwidth: 120kHz
 - Propagation delay: 2μs
 - Response time: 3.7μs
- Operating supply voltage: 4.5V to 5.5V
- Bidirectional and unidirectional current sensing
- -40°C to +125°C Working Ambient Temperature Range
- Robust Galvanic Isolation
 - 5000V_{RMS} withstand isolation voltage
 - 1097V_{RMS} maximum working isolation voltage
 - 10kV maximum surge isolation withstand voltage
- 16-pin wide-body SOIC16 (W) Package
- Safety regulatory approvals
 - 5kV_{RMS} isolation for 1 minute according to UL1577

2. Applications

- Solar Energy
- Motor Control
- EC Charging
- Power supplies

Industrial AC/DC and DC/DC

3. General Description

The CA-IS23050W is a highly accurate and cost-effective current sensor IC suitable for AC/DC current sensing in a variety of industrial, commercial, and communications systems. It features a low-offset, linear Hall sensor circuit and a copper conduction path that generates a magnetic field when current flows through it. The integrated Hall IC senses this magnetic field and converts it into a proportional voltage output, which has a positive slope proportional to the current flowing through the primary copper conduction path. The device senses current differentially, rejecting common-mode fields and improving accuracy in magnetically noisy environments. With its $0.61 \text{m}\Omega$ internal resistance, the primary copper conduction path offers low power loss and high inrush current withstand capability. The CA-IS23050W is available in a 16-pin wide-body SOIC

packages. The CA-IS23050W is rated for operation at working ambient temperatures of -40°C to +125°C.

Device Information

Part Number	Package	Package Size(NOM)
CA-IS23050W	SOIC16-WB	10 mm x 7.5 mm

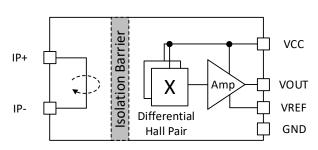


Figure 3-1. Simplified Schematic



4. Ordering Information

Table 4-1. Ordering Information

Part #	Primary Current(A)	Power Supply(V)	Sensitivity(mV/A)	Zero Current Output Voltage(V)	Package
CA-IS23050W	±50	5	40	2.5	SOIC16-WB



Table of Contents

1.	Featu	res				
2.	Applications					
3.		ral Description				
4.		ring Information				
5.		ion History				
6.		onfiguration and Description				
	6.1.	CA-IS23050W Pin Configuration and Description				
7.	Speci	fications				
	7.1.	Absolute Maximum Ratings ¹				
	7.2.	ESD Ratings				
	7.3.	Recommended Operating Conditions				
	7.4.	Thermal Information				
	7.5.	Insulation Specifications				
	7.6.	Safety-Related Certifications				
	7.7.	Common Electrical Characteristics ¹				
	7.8.	Performance Characteristics				
	7.9.	Typical Operating Characteristics				

Deta	iled Description	9	
8.1.	•		
8.2.	Quiescent Output Voltage (V _{OUT(Q)})	9	
8.3.			
8.4.	Power-On Time (t _{PO})	10	
8.5.	Transfer Function	10	
Appl	ication and Implementation	11	
9.1.	Typical Application Circuit	11	
9.2.	PCB Layout	12	
9.	2.1. Layout Guidelines	12	
9.	2.2. Layout example	12	
Pack	age Information	13	
10.1.	16-Pin Wide Body SOIC Package Outline	13	
Solde	ering Temperature (reflow) Profile	14	
12. Tape and Reel Information 1			
Impo	ortant statement	16	
	8.1. 8.2. 8.3. 8.4. 8.5. Appl i 9.1. 9.2. 9. Pack i 10.1. Solde	8.2. Quiescent Output Voltage (VouT(Q)) 8.3. Response Time (tresponse) 8.4. Power-On Time (tpo) 8.5. Transfer Function Application and Implementation 9.1. Typical Application Circuit 9.2. PCB Layout 9.2.1. Layout Guidelines 9.2.2. Layout example Package Information 10.1. 16-Pin Wide Body SOIC Package Outline Soldering Temperature (reflow) Profile	

5. Revision History

Revision Number	Description	Page Changed
Version 1.0	Initial publish	NA



6. Pin Configuration and Description

6.1. CA-IS23050W Pin Configuration and Description

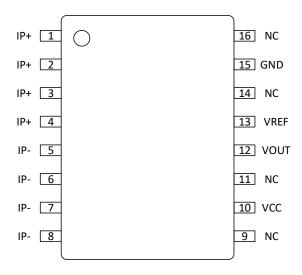


Figure 6-1. The CA-IS23050W Pin Configuration

Table 6-1. The CA-IS23050W Pin Description

Pin Name	Pin Number	Туре	Description
IP+	1-4	Input	Input current positive pin
IP-	5-8	Input	Input current negative pin
NC	9,11,14,16		Reserved. Pin can be connected to GND or left floating
VCC	10	Power Supply	Power supply
VOUT	12	Output	Output voltage
VREF	13	Output	Zero current output voltage reference. Leave pin floating if not used
GND	15	Ground	Ground



7. Specifications

7.1. Absolute Maximum Ratings¹

over operating free-air temperature range unless otherwise specified. ¹

	Parameters	Minimum	Maximum	Unit
V _{CC}	Supply voltage	0	6	V
V_{RCC}	Reverse supply voltage	-0.5	0	V
V _{OUT}	Output voltage	0	6	V
V_{ROUT}	Reverse output voltage	-0.5	0	V
T _A	Operating ambient temperature	-40	125	°C
T _J ²	Junction temperature	-55	165	°C
T _{stg}	Storage temperature	-65	165	°C

Notes:

7.2. ESD Ratings

			Value	Unit
V _{ESD} Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001.	±2000	V	
VE	SD Liectrostatic discharge	Charged device model (CDM), per JEDEC specification JESD22-C101.	±500	V

7.3. Recommended Operating Conditions

Over operating free-air temperature range unless otherwise specified.

	Parameters	Minimum	Typical	Maximum	Unit
V_{CC}	Operating supply voltage	4.5	5	5.5	V
T _A	Ambient temperature	-40		125	°C

7.4. Thermal Information

	Thermal Metric	SOIC16-WB	Unit
i nermai wetric		(W)	Unit
$R_{\theta JA}$	Junction-to-ambient thermal resistance	25	°C/W

7.5. Insulation Specifications

	Parameters	Test Conditions	Specifications W	Unit
Vsurge	Surge voltage	Tested ±5 pulses at 2/minute in compliance to IEC 61000-4-5 1.2 µs (rise) / 50 µs (width)	10	kV
V _{ISO}	Dielectric Strength Test Voltage	Agency type-tested for 60 seconds per UL standard 60950-1 (edition 2); production- tested at VISO for 1 second, in accordance with UL 60950-1 (edition 2).	5000	V _{RMS}
V _{WVBI}	Working Voltage for Basic Isolation	Maximum approved working voltage for basic (single) isolation according to UL 60950-1 (edition 2)	1550	Vpk or VDC
			1097	V_{RMS}
D _{cl}	External Clearance	Minimum distance through air from IP leads to signal leads.	8.2	mm
D _{cr}	External Creepage	Minimum distance along package body from IP leads to signal leads.	8.2	mm
DTI	Distance Through Insulation	Minimum internal distance through insulation	90	μm
CTI	Comparative Tracking Index	Material Group II	400 to 599	V

^{1.} The stresses listed under "Absolute Maximum Ratings" are stress ratings only, not for functional operation condition. Exposure to absolute maximum rating conditions for extended periods may cause permanent damage to the device.

^{2.} To maintain the recommended operating junction temperature conditions, see Thermal Information.





7.6. Safety-Related Certifications

UL(Pending)	TUV(Pending)
Certified according to UL 1577 Component Recognition Program	Certified according to GB 4943.1-2011 and GB 8898-2011



7.7. Common Electrical Characteristics¹

All minimum/maximum specs are at $T_A = -40$ °C to +125°C, $V_{CC} = 5V$, unless otherwise noted.

	Parameters	Test Conditions	Minimum	Typical	Maximum	Unit
POWER			•			
V _{CC}	Supply Voltage		4.5	5.0	5.5	V
I _{CC}	Supply Current	VCC=5V, output open	11.5	14.0	16.0	mA
t _{po}	Power-on Time	T _A = 25°C		78.0		μs
V _{UVLOH}	UVLO voltage threshold	VCC rising		3.8	4.1	V
V _{UVLOL}	UVLO voltage threshold	VCC falling	2.9	3.2		V
Output	Satge					
CL	Output Capacitance Load	VOUT to GND		1.0	10.0	nF
R _L	Output Resistive Load	VOUT to GND and VOUT to VCC	4.7			kΩ
R _{REF}	VREF Resistive Load	VREF to GND and VREF to VCC	100			kΩ
t _r	Rise Time	T _A = 25°C, C _L = 1 nf		3.6		μs
t _{pd}	Propagation Time	T _A = 25°C, C _L = 1 nf		2.0		μs
t _{response}	Response Time	$T_A = 25^{\circ}C, C_L = 1 \text{ nf}$	3.0	3.7		μs
SR	Output Slew Rate	$T_A = 25^{\circ}C, C_L = 1 \text{ nf}$		0.4		V/µs
V _{REF_INI}	Reference Output Voltage		2.48	2.5	2.52	V
V _{SAT(H)}	High Output Saturation Soltage ²	$R_{L(DOWN)} = 10k\Omega$ to GND	4.7			V
V _{SAT(L)}	Low Output Saturation Voltage ²	$R_{L(UP)} = 10k\Omega$ to VCC			0.3	V
Input St	age					
R _{IP}	Primary Conductor Resistance	T _A = 25°C		0.61		mΩ
L _{IP}	Primary Conductor Inductance	T _A = 25°C		2		nH
CMFRR	Common Mode Field Rejection Ratio	Uniform external magnetic field		70		dB
Accurac	y and Frequency					
BW	Frequency Bandwidth	Small signal -3 dB; C _L = 1 nF		120		kHz
	Noise	Input-referenced noise: C _F = 4.7 nF,		100		mA _{RMS}
I _N	NOISE	$C_L = 1 \text{ nF, BW} = 18 \text{ kHz, } T_A = 25^{\circ}\text{C}$		100		
E _{LIN}	Nonlinearity	Over full range of I _P		±0.2	±1	%
E _{SYM}	Symmetry	Over full range of I _P		±0.2	±1	%

Notes:

7.8. Performance Characteristics

All minimum/maximum specs are at $T_A = -40$ °C to +125°C, $V_{CC} = 5V$, unless otherwise noted.

	Parameters	Test Conditions	Minimum	Typical ¹	Maximum	Unit				
Nominal Performance										
I _{PR}	Current-sensing Range		-50	-50		Α				
Sens	Sensitivity	Over full range of I _P , T _A = 25°C		40		mV/A				
V _{OUT(Q)} Zero Current Output Voltage		Bidirectional; I _P = 0 A, T _A = 25°C	2.49	2.5	2.51	V				
Accuracy Performance										
_	Total Output Error ²	I _P =I _{PR(max)} , T _A = 25°C to 125°C	-3		3	%				
E _{TOT}	iotai Output Error	$I_P = I_{PR(max)}$, $T_A = -40^{\circ}$ C to 25°C	-1		4.5	%				
Total Output Error Components ³ $E_{TOT} = E_{SENS} + 100 \times V_{OE}/(Sens \times I_P)$										
_	Considiuity France	I _P =I _{PR(max)} , T _A = 25°C to 125°C	-2.5		2.5	%				
E _{sens}	Sensitivity Error	$I_P = I_{PR(max)}$, $T_A = -40^{\circ}$ C to 25°C	-0.5		4.0	%				
V	Voltage Officet France	I _P =0 A, T _A = 25°C to 125°C	-10		20	mV				
V_{OE}	Voltage Offset Error	I _P =0 A, T _A = -40°C to 25°C	-10		10	mV				

^{1.} Device may be operated at higher primary current levels, I_P , ambient temperatures, T_A , and internal leadframe temperatures, provided the Maximum Junction Temperature, T_J (max), is not exceeded.

^{2.} The sensor IC will continue to respond to current beyond the range of I_P until the high or low output saturation voltage; however, the nonlinearity in this region will be worse than through the rest of the measurement range.



CA-IS23050W

Version 1.0

Shanghai Chipanalog Microelectronics Co., Ltd.

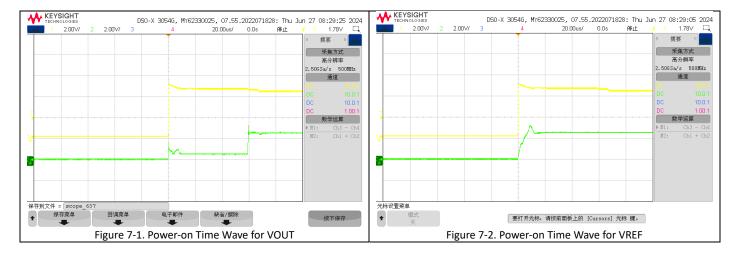
Life Time Drift Characteristics								
E _{sens_drift} Sensitivity Error Lifetime Drift		±1	%					
E _{tot_drift} Total Output Error Lifetime Drift		± 1	%					

Notes:

- 1. Typical values with \pm are 3 sigma values.
- 2. Percentage of I_P , with $IP=I_{PR(max)}$.
- 3. A single part will not have both the maximum/minimum sensitivity error and maximum/minimum offset voltage, as that would violate the maximum/minimum total output error specification. Also, 3 sigma distribution values are combined by taking the square root of the sum of the squares.

7.9. Typical Operating Characteristics

All values are at V_{CC} = 5V, C_L = 1nF, unless otherwise noted.



8. Detailed Description

8.1. Overview

The CA-IS23050W current sensor are based on the Hall principle and can accurately measure AC/DC current while minimizing measurement costs. This sensor finds extensive use in various current monitoring applications, including consumer, industrial, and automotive scenarios. Compared to current transformers, the CA-IS23050W offers a compact size, which can significantly reduce PCB size. In comparison to shunt resistor + isolated amplifier solutions, the CA-IS23050W only requires low-side power supply, eliminating the complexity of high-side power supply design.

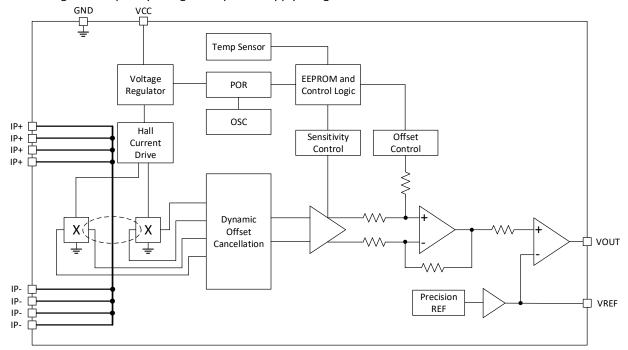


Figure 8-1. Functional block diagram

The internal conductor of the CA-IS23050W generates a magnetic field proportional to the current value, according to Maxwell's equations. The sensor converts this magnetic field value into a voltage output, ensuring a high level of accuracy. Moreover, the sensor has an ultra-small resistor value, ensuring little influence on thermal power consumption.

8.2. Quiescent Output Voltage (Vout(Q))

The quiescent output voltage $V_{\text{OUT}(Q)}$ of the CA-IS23050W indicates the output voltage of the IC when there is no magnetic field. Although the theoretical output voltage of the CA-IS23050W is 2.5V, factors such as offset voltage, sensitivity, packaging stress, and temperature coefficient may cause the actual quiescent output voltage to deviate from the theoretical figure. During factory testing, the actual quiescent voltage is modified to be within ± 10 mV of the theoretical value. The quiescent output voltage is also influenced by the temperature coefficient, which means that as the temperature changes, the quiescent output voltage will also change (this effect is more noticeable when sensitivity is higher). The CA-IS23050W is equipped with temperature sensors that can modify the temperature coefficient of the quiescent output voltage.

8.3. Response Time (tresponse)

Response Time is a term used to define the time difference between the moment when the magnetic field reaches 80% of its target value and the moment when the output voltage of the IC reaches 80% of its target value. This difference is measured and expressed in micro seconds. The Response Time is related to the sensitivity of the IC and the size of the output load capacitance. It is an important parameter to consider when using magnetic sensors, especially in applications where a quick response is



required. The accuracy of the Response Time measurement is crucial to ensure reliable and precise operation of the sensor in various conditions.

8.4. Power-On Time (t_{PO})

Power-On Time is a term used to define the time required for the output voltage of a sensor to reach 90% of its target value after the supply voltage reaches 4.5V, at a specific magnetic field strength. This time difference is measured and expressed in micro seconds. The Power-On Time is an important parameter to consider when using magnetic sensors, especially in applications where a quick response is required. The accuracy of the Power-On Time measurement is crucial to ensure reliable and precise operation of the sensor in various conditions.

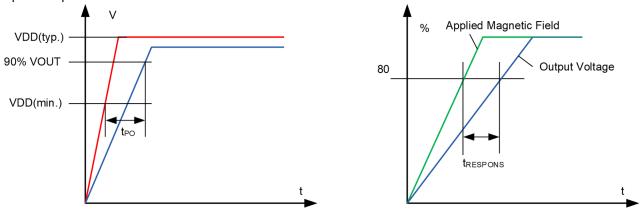


Figure 8-2. Power-On Time and Response Time

8.5. Transfer Function

The ideal first-order transfer function of the CA-IS23050W is given by Equation 1, where the output voltage V_{OUT} is a linear function of input current I_P . The accuracy of the device is quantified both by the error terms in the transfer function parameters, as well as by nonidealities that introduce additional error terms not in the simplified linear model.

$$V_{OUT} = (I_P \times Sens) + V_{REF}$$

Where

- V_{OUT} is the output voltage.
- I_P is the isolated input current.
- Sens is the sensitivity of the CA-IS23050W.
- V_{REF} is the zero current reference output voltage.

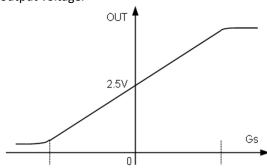


Figure 8-3. Transfer Function



9. Application and Implementation

9.1. Typical Application Circuit

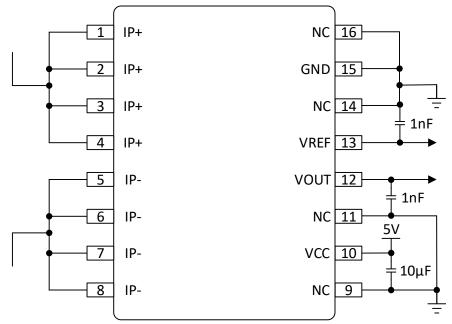


Figure 9-1. Single-end output application

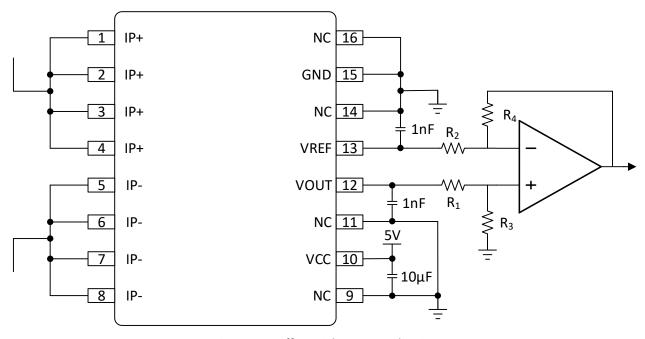


Figure 9-2. Differential output application



9.2. PCB Layout

9.2.1. Layout Guidelines

The CA-IS23050W is specified for a continuous current handling capability on the EVM which uses 4oz copper planes. This current capability is fundamentally limited by the maximum device junction temperature and the thermal environment, primarily the PCB layout and design. To maximize current-handling capability and thermal stability of the device, take care with PCB layout and construction to optimize the thermal capability. Efforts to improve the thermal performance beyond the design and construction of the EVM can result in increased continuous-current capability due to higher heat transfer to the ambient environment. Keys to improving thermal performance of the PCB include:

- Use large copper planes for both input current path and isolated power planes and signals.
- Use heavier copper PCB construction.
- Place thermal via farms around the isolated current input.
- Provide airflow across the surface of the PCB.

9.2.2. Layout example

An example layout, shown in Figure 9-3, is from the EVM User's Guide. Device performance is targeted for thermal and magnetic characteristics of this layout, which provides optimal current flow from the terminal connectors to the device input pins while large copper planes enhance thermal performance.

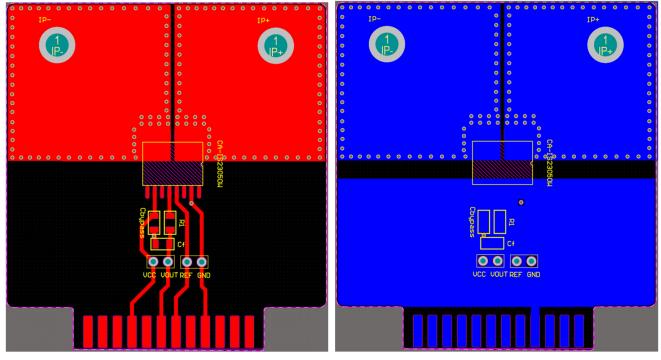
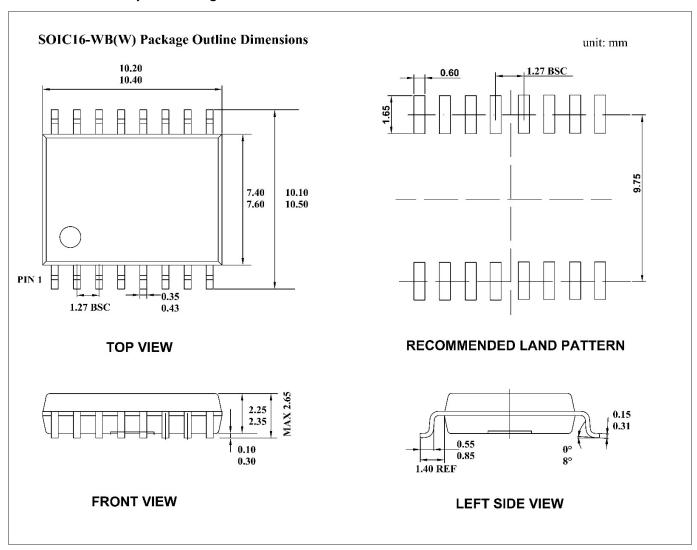


Figure 9-3. Recommended Board Layout



10. Package Information

10.1. 16-Pin Wide Body SOIC Package Outline



Note:

1. All dimensions are in millimeters, angles are in degrees.

.



11. Soldering Temperature (reflow) Profile

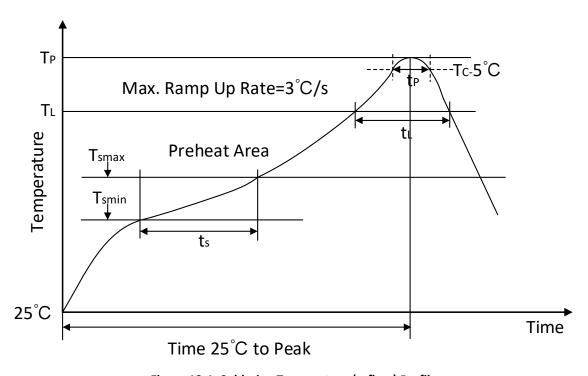


Figure 12-1. Soldering Temperature (reflow) Profile

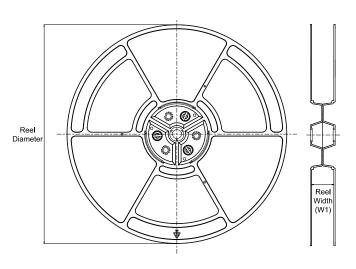
Table 12-1. Soldering Temperature Parameter

Profile Feature	Pb-Free Assembly
Average ramp-up rate(217 C to Peak)	3 ℃/second max
Time of Preheat temp(from 150 ℃ to 200 ℃	60-120 second
Time to be maintained above 217 °C	60-150 second
Peak temperature	260 +5/-0 ℃
Time within 5 ℃ of actual peak temp	30 second
Ramp-down rate	6 C/second max.
Time from 25 C to peak temp	8 minutes max

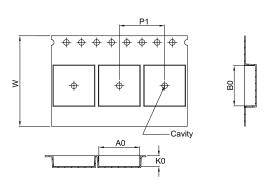


12. Tape and Reel Information

REEL DIMENSIONS

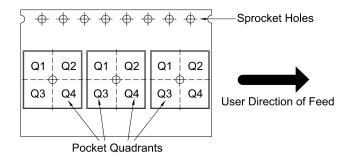


TAPE DIMENSIONS



Α0	Dimension designed to accommodate the component width					
В0	Dimension designed to accommodate the component length					
K0	Dimension designed to accommodate the component					
	thickness					
W	Overall width of the carrier tape					
P1	Pitch between successive cavity centers					

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CA-IS23050W	SOIC	W	16	1000	330	16.40	10.90	10.70	3.2	12.00	16.00	Q1



13. Important statement

The above information is for reference only and used for helping Chipanalog customers with design, research and development. Chipanalog reserves the rights to change the above information due to technological innovation without advance notice.

All Chipanalog products pass ex-factory test. As for specific practical applications, customers need to be responsible for evaluating and determining whether the products are applicable or not by themselves. Chipanalog's authorization for customers to use the resources are only limited to development of the related applications of the Chipanalog products. In addition to this, the resources cannot be copied or shown, and Chipanalog is not responsible for any claims, compensations, costs, losses, liabilities and the like arising from the use of the resources.

Trademark information

Chipanalog Inc.® and Chipanalog® are registered trademarks of Chipanalog.



http://www.chipanalog.com